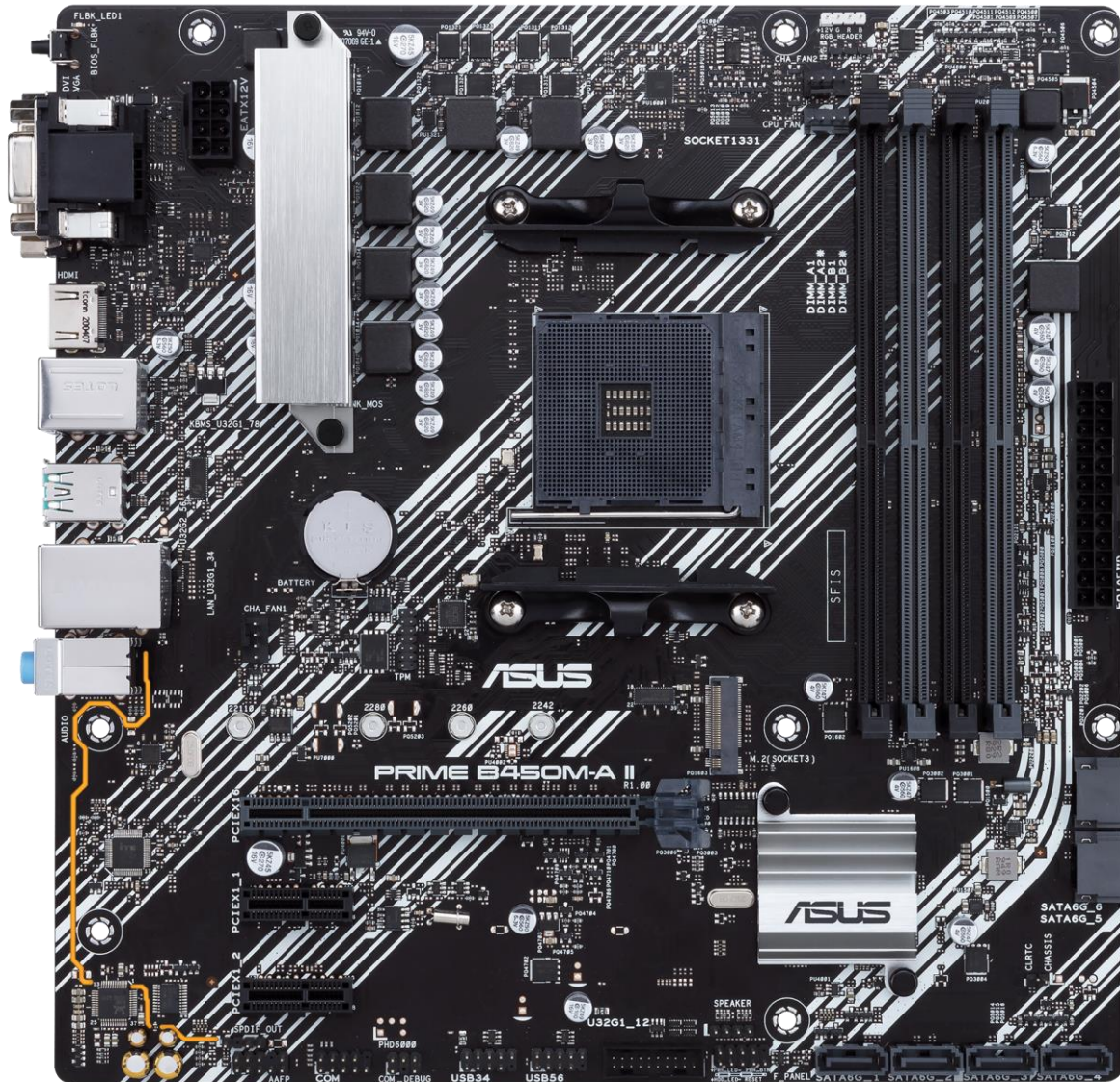


## 1. STANDARD APPEARANCE

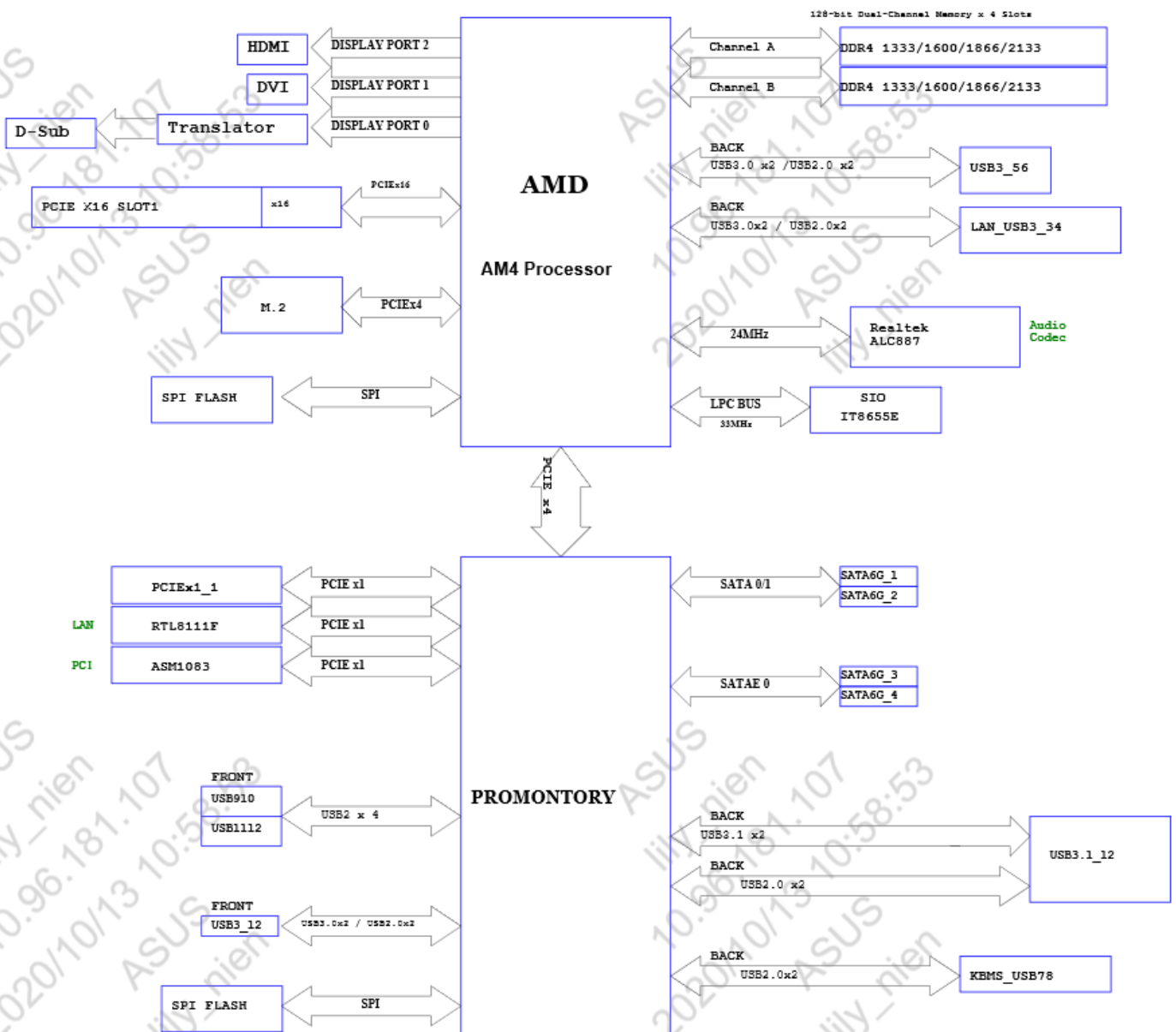


## 2. BLOCK DIAGRAM

### AMD AM4 GOLDEN

Rev 1.00

2016.03.09



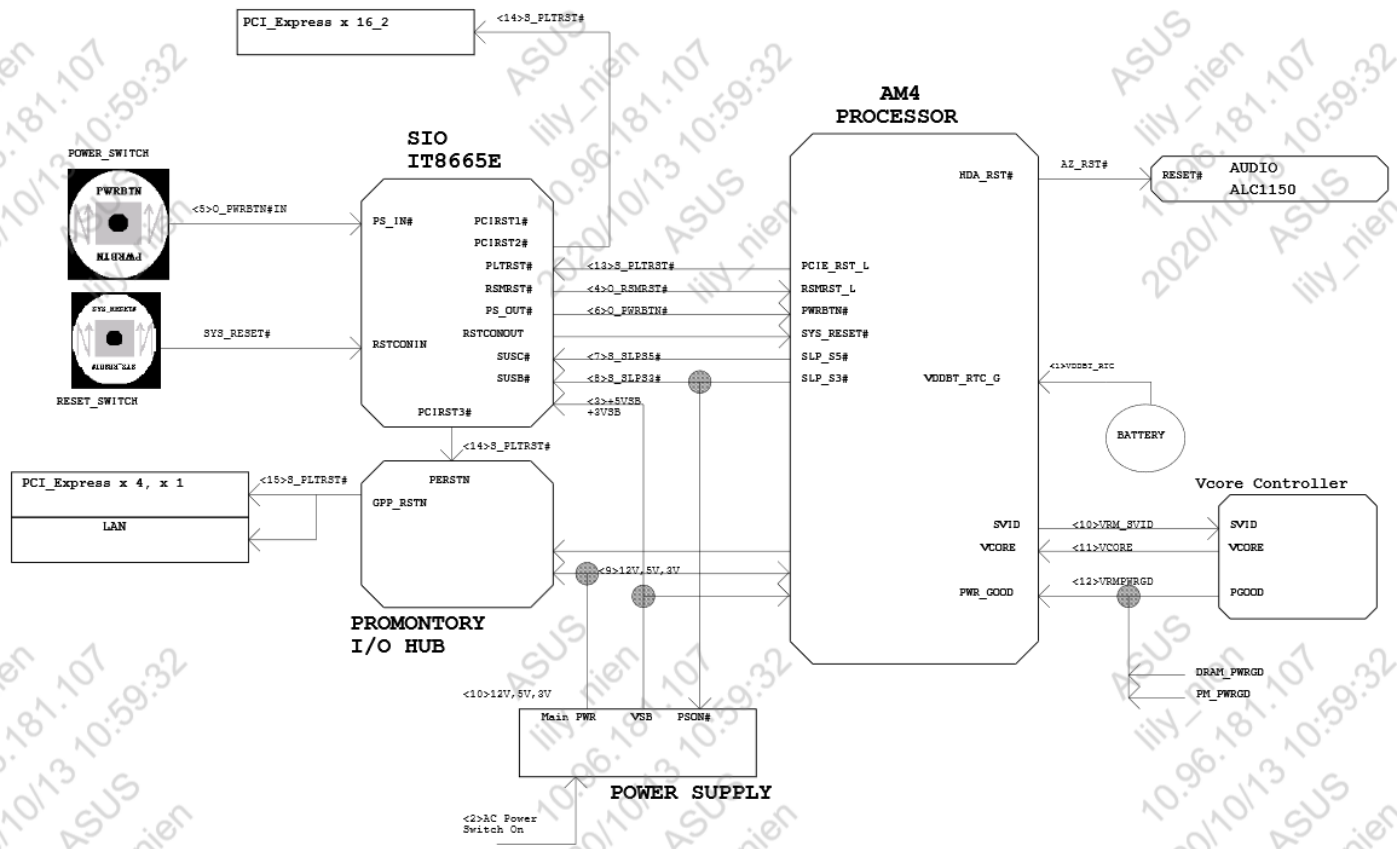
The image displays three schematic diagrams of power distribution networks (PDNs) for a system, likely a server or industrial PC, showing the flow of power from input rails to various components and output rails.

**Top Diagram:** This diagram shows the power distribution from the +12V\_CPU and +5V rails. The +12V\_CPU rail is connected to the CPU (0.75-1.5V (80A)) and VDDSOC (0.75-1.2V (80A)). The +5V rail is connected to the NTMF S4C10-EMB20P05A, which provides +5VSB to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)). The +5VSB rail is also connected to the RT1220G0W, which provides +5VSB to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)). The +5VSB rail is also connected to the RT1220G0W, which provides +5VSB to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)).

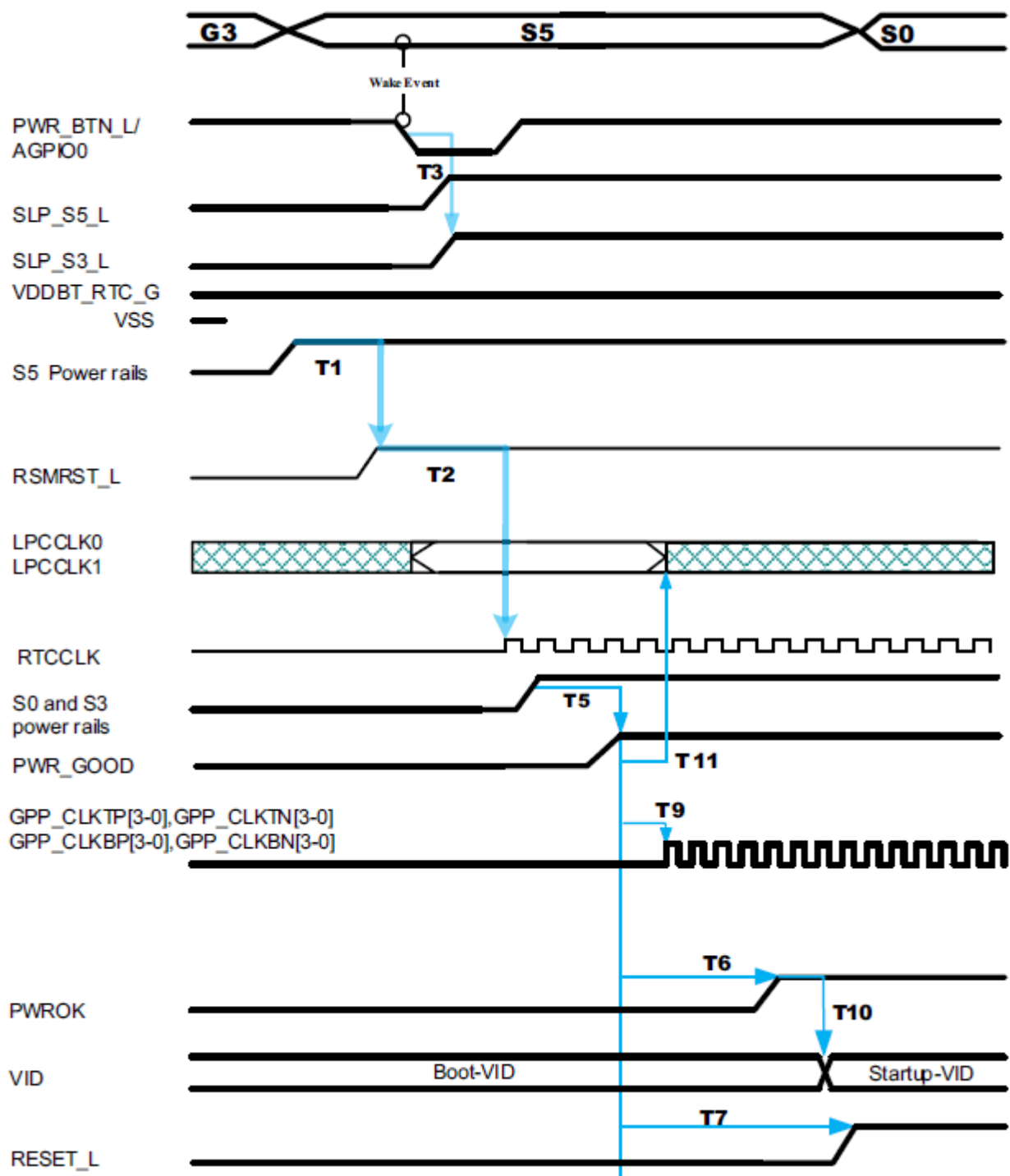
**Middle Diagram:** This diagram shows the power distribution from the +5VSB\_ATX rail. The +5VSB\_ATX rail is connected to the NTMF S4C10-EMB20P03P, which provides +5VSB\_DUAL to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)). The +5VSB\_DUAL rail is also connected to the TP35120G0W, which provides +5VSB to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)).

**Bottom Diagram:** This diagram shows the power distribution from the +3VSB\_ATX and +3VSB rails. The +3VSB\_ATX rail is connected to the U2200S, which provides +3VSB to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)). The +3VSB rail is connected to the UP800S04M4S, which provides +3VSB to the CPU (0.75-1.2V (80A)) and VDDSOC (0.75-1.2V (80A)).

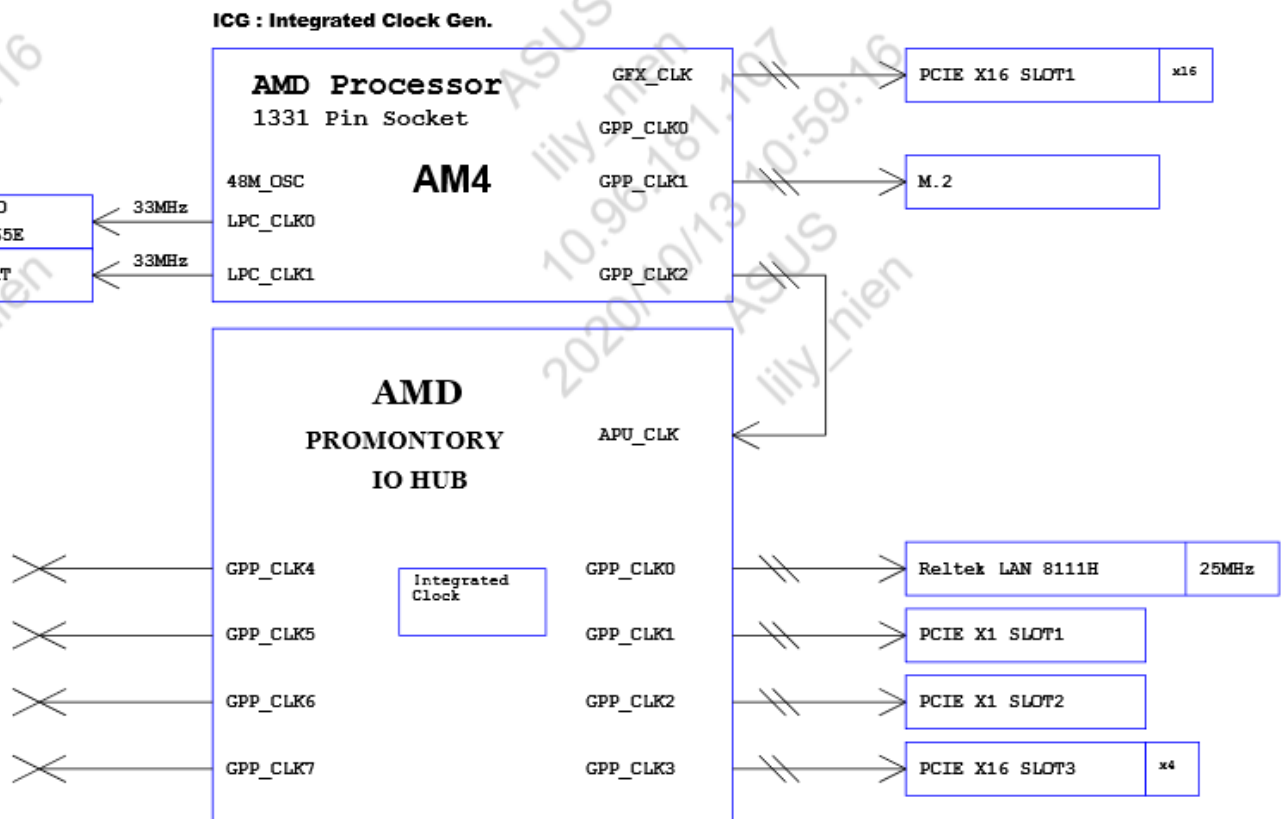
## 4. POWER ON SEQUENCE



## 5. Timing Diagram for G3 to S0

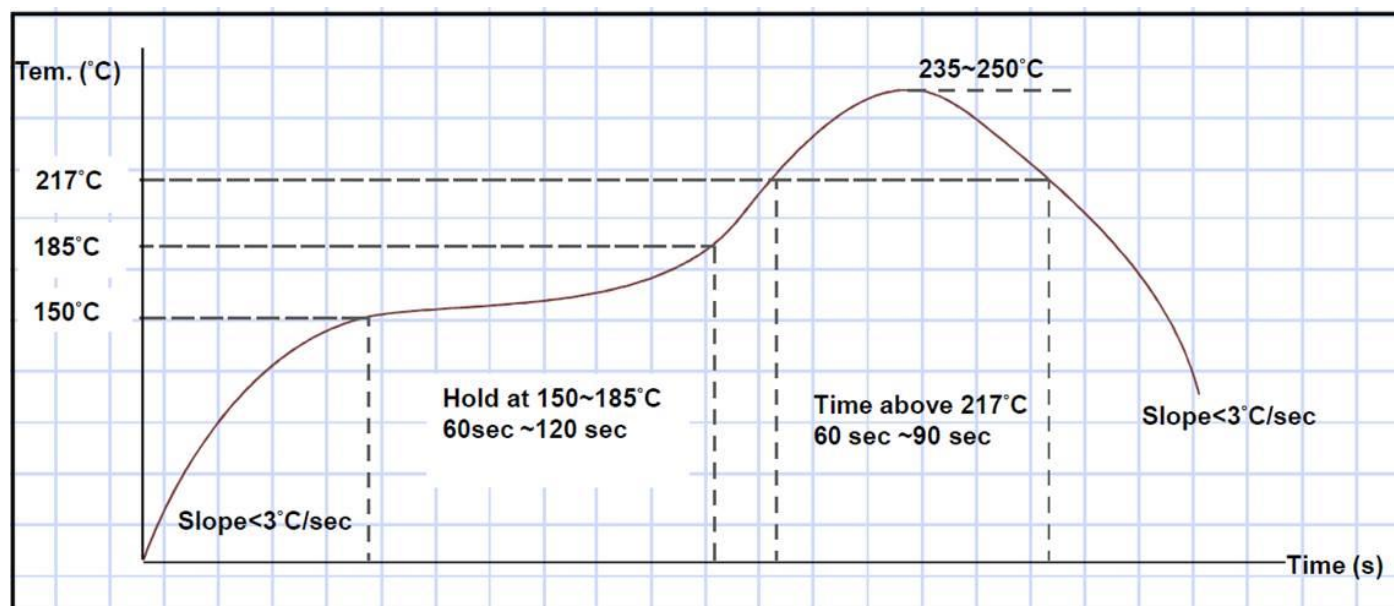


## 6. Frequency Flow





## 7. Socket reflow profile



Profile Feature	SMT Component Vendor Spec
Preheat/Soak	150 °C
Temperature Min (T <sub>min</sub> )	200 °C
Temperature Max (T <sub>max</sub> )	need endure 120 seconds
Time (ts) from (T <sub>min</sub> to T <sub>max</sub> )	
Ramp-up rate (TL to Tp)	need endure 3 °C/second max.
Liquidous temperature (TL)	217 °C
Time (tl) maintained above TL	need endure 90 seconds
Peak package body temperature (Tp)	260 °C
Time (tp)* within 5 °C of the specified classification temperature (Tc), see Figure 1-1 .	need endure 10* seconds
Ramp-down rate (Tp to TL)	need endure 6 °C/second max.
Time 25 °C to peak temperature	need endure 8 minutes max.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within  $\pm 2^{\circ}C$  of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2 : For SMT type component, it need be able to withstand twice times SMT Reflow + once DIP Wave soldering process.